Hybrid Synaptic Devices Employing Combined Ferroelectric and Charge-Trapping Mechanisms for Neuromorphic Computing

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The conventional von-Neumann architecture suffers from fatal bottlenecks because it separates memory and logic processes. To overcome this limitation, intensive research is being conducted on neuromorphic computing. [1]

Synaptic devices are required to exhibit continuous weight states and to support linear and symmetric weight modulation under low operating voltages in response to input signals. To achieve these characteristics, charge-trapping, ferroelectric, and phase-change devices have been extensively studied as potential candidates for synaptic devices. In this study, we propose a hybrid synaptic device employing combined ferroelectric and charge-trapping mechanisms for neuromorphic computing.

A ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layer was deposited via DPALD and then a HfO_2 layer was deposited on HZO as a capping layer to stabilize the ferroelectric phase of HZO and a charge-trapping layer. By combining fast-switching ferroelectrics with stable modulation of charge trapping, the proposed device achieves balanced performance in speed, linearity, retention, and symmetry, all of which are required for synaptic applications.

To investigate the effects of HfO_2 thickness and annealing conditions on device characteristics, we fabricated a synaptic capacitor with a 1-nm-thick HfO_2 layer exhibiting a remanent polarization (2Pr) value of 9.51 μC/cm² and counterclockwise hysteresis indicating the dominance of ferroelectric polarization. In contrast, a synaptic transistor with a 2-nm-thick HfO_2 layer annealed at 500 °C exhibited a 2Pr value of 5.51 μC/cm² with clockwise hysteresis indicating the dominance of charge-trapping. These results demonstrate that polarization and charge-trapping mechanisms compete within the device and that synaptic characteristics can be optimized by adjusting the thickness of HfO_2 and annealing conditions.

Furthermore, both devices exhibited long-term memory (LTM) behavior in response to a single pulse. Under multiple pulses, the synaptic capacitor exhibited long-term potentiation (LTP), while the synaptic transistor exhibited long-term depression (LTD). These results confirm the potential of the proposed structures as artificial synaptic devices capable of supporting learning and memory functions for neuromorphic applications.

In summary, this study demonstrates that the hybrid structure, which combines ferroelectric and charge-trapping mechanisms, can overcome the limitations of single-mechanism devices and enable reliable implementation of artificial synapses.

References

[1] J. W. Lim, M. A. Park, and J. Kim, "Photo-synaptic oxide transistors with Al_2O_3/SiO_x stacked gate dielectric exhibiting 1024 conduction states with good linearity," *Adv. Electron. Mater.*, vol. 8, no. 10, Art. no. 2200494, Oct. 2022, doi: 10.1002/aelm.202200494.

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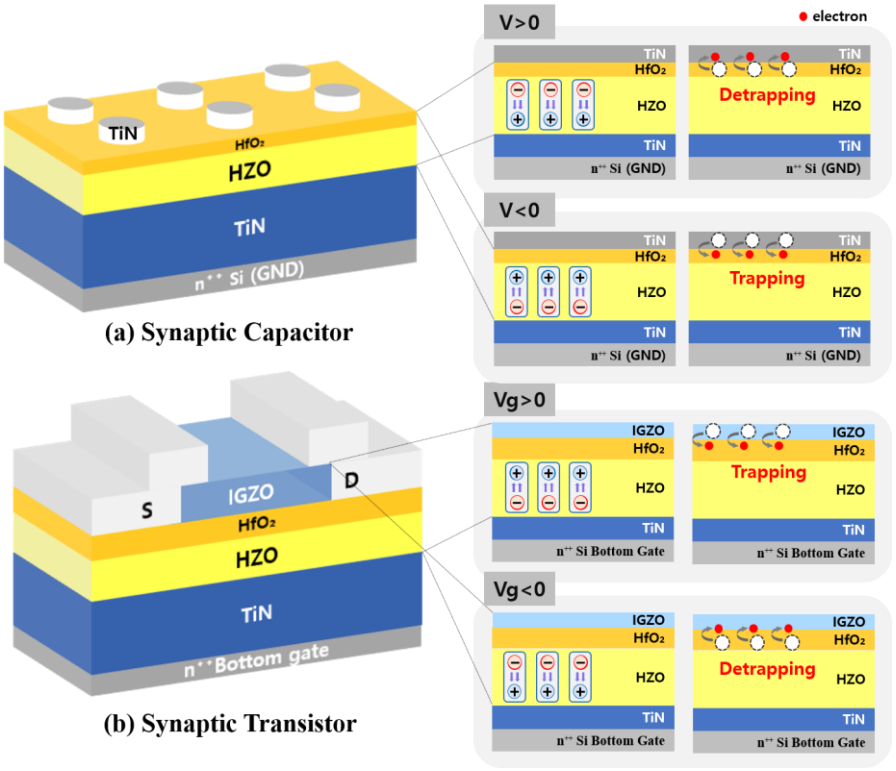

Figure 1. Schematic diagrams for the fabricated (a) two-terminal synaptic capacitor and (b) three-terminal synaptic transistor, along with their operating mechanisms under various bias conditions.

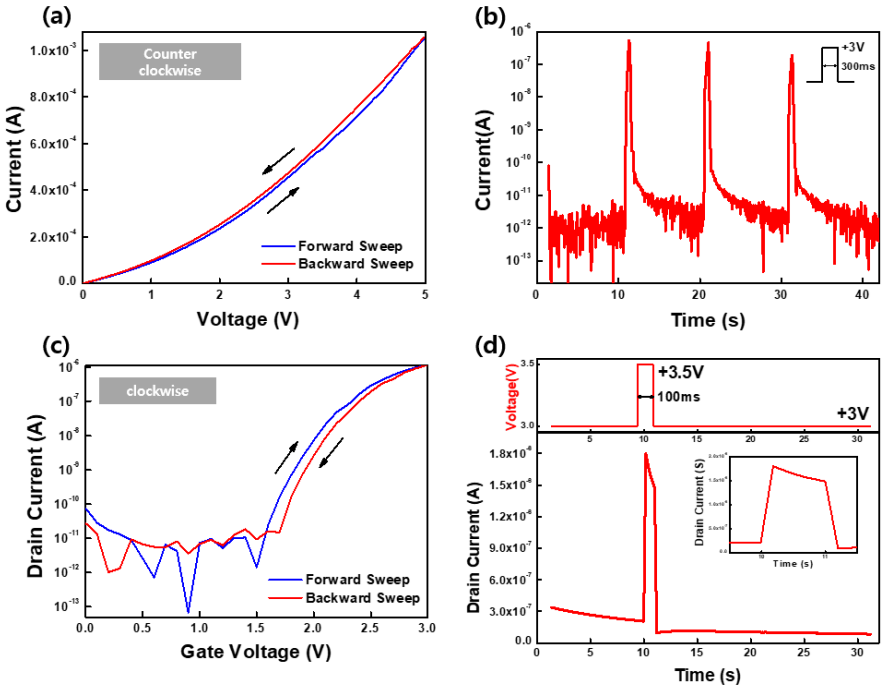

Figure 2. (a) Transfer curves of the synaptic capacitor exhibiting counterclockwise hysteresis under forward and reverse bias sweeps. (b) LTM characteristics of the synaptic capacitor induced by discrete voltage pulse stimuli. (c) Transfer curves of the synaptic transistor exhibiting clockwise hysteresis under forward and reverse bias sweeps. (d) LTM characteristics of the synaptic transistor induced by discrete voltage pulse stimuli.